Please amend Claim 2, as follows:

2. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a first insulating film formed over said semiconductor substrate;

a first conducting plug formed in said first insulating film;

a storage electrode formed over said first insulating film, and electrically connected to said conducting plug;

a capacitor dielectric film formed over said storage electrode;

an opposing electrode formed over said capacitor dielectric film, and having an extension extending over said first insulating film;

a second insulating film formed over said opposing electrode;

a first contact hole formed through said second insulating film and said extension of the opposing electrode; and

a first conductor pattern burying said contact hole.

Please amend Claim 18, as follows:

18. (Amended) The semiconductor memory device according to claim 17, wherein said bit line includes a conducting bit layer, oxide side walls on side walls of the conducting bit layer, and a bit silicon nitride layer covering the conducting bit layer and the oxide side walls of the bit line.

Please add new Claims 24-37, as follows:

24. The semiconductor device according to claim 1, further comprising:

a wiring layer formed on the semiconductor substrate and covered with said first insulating film;

a second contact hole formed through said first and second insulating films to reach a surface of said wiring layer; and

a second conductor pattern burying said second contact hole.

25. The semiconductor device according to claim 24, further comprising:

an impurity diffusion region formed in said semiconductor substrate and connected to said wiring layer;

a third contact hole formed through said second and first insulating film, and reaching said impurity diffusion region; and

a third conductive pattern burying said third contact hole.

26. The semiconductor device according to claim 25, further comprising:

a switching transistor including an insulated gate formed on the substrate, and covered with said first insulating film, and source/drain regions formed in the substrate on both sides of the insulated gate; and

a first conductive plug formed through the first insulating film and connected to said one electrode of the capacitor and one of said source drain regions.

27. The semiconductor device according to claim 26, wherein said insulated gate comprises a gate insulating layer formed on the semiconductor substrate, a gate silicon layer formed on the gate insulating layer, a gate silicide layer formed on the gate silicon layer, oxide side walls formed on side surfaces of the gate silicon layer and the gate silicide layer, and a gate silicon nitride layer covering the gate silicon layer and the oxide side walls.

28. The semiconductor memory device according to claim 27, wherein said first conducting plug is contiguous to the gate silicon nitride layer.

29. The semiconductor memory device according to claim 28, further comprising:

a second conducting plug formed through said first insulating film and connected to another of said source/drain regions; and

a bit line formed over the first insulating film and in the second insulating film and connected to said second conducting plug.

30. The semiconductor memory device according to claim 29, wherein said bit line includes a conducting bit layer, oxide side walls on side walls of the conducting bit layer, and a bit silicon nitride layer covering the conducting bit layer and the oxide side walls of the bit line.

31. The semiconductor device according to claim 2, further comprising:

a wiring layer formed on the semiconductor substrate and covered with said first insulating film;

a second contact hole formed through said first and second insulating films to reach a surface of said wiring layer; and

a second conductor pattern burying said second contact hole.

32. The semiconductor device according to claim 31, further comprising:

an impurity diffusion region formed in said semiconductor substrate and connected to said wiring layer;

a third contact hole formed through said second and first insulating film, and reaching said impurity diffusion region; and

a third conductive pattern burying said third contact hole.

33. The semiconductor device according to claim 32, further comprising:

a switching transistor including an insulated gate formed on the substrate, and covered with said first insulating film, and source/drain regions formed in the substrate on both sides of the insulated gate;

wherein said first conducting plug is formed through the first insulating film and electrically connected to one of said source/drain regions.

34. The semiconductor device according to claim 33, wherein said insulated gate comprises a gate insulating layer formed on the semiconductor substrate, a gate silicon layer formed on the gate insulating layer, a gate silicide layer formed on the gate silicon layer, oxide side walls formed on side surfaces of the gate silicon layer and the gate silicide layer, and a gate silicon nitride layer covering the gate silicon layer and the oxide side walls.

35. The semiconductor memory device according to claim 34, wherein said first conducting plug is contiguous to the gate silicon nitride layer.

36. The semiconductor memory device according to claim 35, further comprising:

a second conducting plug formed through said first insulating film and connected to another of said source/drain regions; and

a bit line formed over the first insulating film and in the second insulating film and connected to said second conducting plug.

37. The semiconductor memory device according to claim 36, wherein said bit line includes a conducting bit layer, oxide side walls on side walls of the conducting bit layer, and a bit silicon nitride layer covering the conducting bit layer and the oxide side walls of the bit line.